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January 11, 2001 — Jacqueline Shepherd
Date — Jacqueline Shepherd

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Shin Hwa Li and Annie Tissier
Application No	:	09/632,388
Filed	:	August 3, 2000
For	:	A SEMICONDUCTOR STRUCTURE HAVING AN IMPROVED PRE-METAL DIELECTRIC STACK AND METHOD FOR FORMING THE SAME
Art Unit	:	2823
Docket No.	:	98-P-009C1 (850063.529C1)
Date	:	January 10, 2001

Assistant Commissioner for Patents
Washington, DC 20231

AMENDMENT AND RESPONSE TO RESTRICTION REQUIREMENT

Assistant Commissioner for Patents:

In response to the Restriction Requirement dated December 19, 2000, applicants hereby elect Group I, claims 1-10, for examination at this time.

In view of the above election, applicants hereby cancel claims 11-19 without prejudice to the filing of any divisional, continuation, or continuation-in-part application.

Additionally, please cancel claims 5 and 8 without prejudice and amend claims 1, 3, 4, 6, 9 and 10, as follows:

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1. (Amended) A semiconductor structure, comprising:

a substrate;

a patterned oxide layer disposed over the substrate;

a layer of undoped silicate glass disposed over the patterned oxide layer;

a layer of borophosphorous silicate glass over the layer of undoped silicate glass;

[and]

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a planarized layer of plasma-enhanced tetraethyl orthosilicate over at least a portion of the layer of the borophosphorous silicate glass, and not overlaying at least a portion of the borophosphorous silicate glass layer; and

a layer of plasma-enhanced tetraethyl orthosilicate overlaying the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with at least a portion of the borophosphorous silicate glass region, the layers of the undoped silicate glass, borophosphorous silicate glass, planarized plasma-enhanced tetraethyl orthosilicate and second plasma-enhanced tetraethyl orthosilicate layer together forming a pre-metal dielectric stack.

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3. (Amended) The structure of claim 1 wherein the second layer of plasma-enhanced tetraethyl orthosilicate is planar.

4. (Amended) The structure of claim 3 wherein a combined thickness of the oxide layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the second layer of plasma-enhanced tetraethyl orthosilicate is less than approximately 15k angstroms.

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6. (Amended) An integrated circuit, comprising:

a substrate;

a dielectric layer disposed on the substrate;

a layer of undoped silicate glass disposed on the dielectric layer;

an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass; [and]

a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, the planar dielectric layer directly overlaying at least a portion of the borophosphorous silicate glass and leaving exposed so as to not directly overlay at least a portion of the borophosphorous silicate glass; and

a dielectric layer disposed on the planar dielectric layer and the portions of the borophosphorous silicate glass which are not overlaid by the planar dielectric layer, the layers of undoped silicate glass, borophosphorous silicate glass, [and] planar dielectric layer, and a second dielectric layer together composing a pre-metal dielectric stack.

9. (Amended) The integrated circuit of claim 6 wherein the second dielectric layer is[, further comprising:

a layer of] tetraethyl orthosilicate [disposed on the planar dielectric layer; and

wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate].

10. (Amended) The integrated circuit of claim 6 wherein the second dielectric layer is[, further comprising:

a layer of] plasma-enhanced tetraethyl orthosilicate disposed on the planar dielectric layer; and

wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

Consideration of the elected claims is now requested.

Respectfully submitted,
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